Low-Power Digital Receiver Structure for Multi-Speed HART

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Abstract

This paper presents a low-power digital receiver structure for multi-speed HART which can adaptively demodulate input signal modulated in non-coherent HART FSK or coherent HART C8PSK. A new kind of CSD coded preset equalizer is introduced according to the characteristic of HART channel distortion. Synchronization is divided into initialization stage and tracking stage. In initialization stage, it attains equilibrium state quickly and reduces tracking computation rate, while in tracking stage, it is time-divided carried out and reduces the computation rate of the equalizer and interpolator. Additionally, a novel algorithm is developed for HART FSK demodulation reusing the resource as HART C8PSK. Power consumption can dramatically decrease, because Multiplications used per one symbol demodulation are dramatically reduced; while simulations show that the proposed structure can convergence fast and work very well in low SNR.

Keywords: *Multi-Speed HART, Low-power, CSD Coded Preset Equalizer, Synchronizer, FSK*

1. Introduction

HART (Highway Addressable Remote Transducer) is the global standard that enhances traditional 4-20 signaling by simultaneously allowing two way digital communications, and the global installed base of HART-enabled devices is the largest of all communication protocols at more than 20 million. There are two types of hybrid HART communication protocols, HART FSK and HART C8PSK. HART FSK underlies Bell-202 Telecomm standard, while HART C8PSK is similar to the signaling specified in the CCITT V.27 Telecomm standard. A summary comparison of the two protocols' digital communication is given in table 1.

Table 1: digital communication comparison of the two HART protocols

protocol	Modulation type	Signal rate	Carrier frequency	preamble	Symbol mapping
FSK	Binary FSK	1200baud/s 1200bit/s	1700Hz	40 symbols 1	0=2200Hz;1=1200Hz
C8PSK	Coherent 8-ary PSK	3200baud/s 9600bit/s	3200Hz	40 Cyclic symbols 6,2	0=13 π /8;1=15 π /8; 2=11 π /8; 3=7 π /8;4=5 π /8; 5=7 π /8 6=3 π /8;7= π /8

The physical device type, message structure and the network configuration rules of HART C8PSK are defined as the same as HART FSK, which means HART C8PSK can, replace or co-exist with HART FSK using the same topology, cabling, and device circuits. Some industry giant, such as Rosemount, SMAR, and Siemens, organized by HCF (HART communication Foundation), joined together developing a MSH (Multi-Speed HART, also referred as High speed HART, HSH) modem chip when HART C8PSK protocol established. However, it did not applied in industry because of high power consumption [1]. An Austria company, called Volker Schindler, made a MSH chip in 2009, power of which was a little lower than the power limitation, but still higher than applicable level [2].

The C8PSK band extends from 800 Hz to 5600 Hz, while the HART FSK band from 900 to 2500 Hz. According to HCF, the HART channel (network) is thought to cause a signal-pole low-pass filter with roll-off range from 3.7 kHz to 10 kHz, and the pole frequency varies as the network characteristics

change [3]. Though the HART FSK signals distort little during transmission, MSH needs an adaptive equalization compensate for cable losses. Coherent demodulation can provide about 3 dB better SNR than no-coherent demodulation algorithms [4] and HART C8PSK protocol specifies MSH receiver must use coherent demodulation, so AGC (Automatic Gain Control), pulse shaping filter, symbol synchronization, carrier recovery, and signal identification should be provided within a MSH receiver modem. The difficulty to develop a MSH modem chip is how to encapsulate the complexity of the two kinds of signals and adaptively demodulate both types of signals while keep the power consumption low. The transmitter part of the MSH modem is relatively simpler and its power consumption is low, so we focus our attention on the receiver part of MSH modem only.

Software defined radio [5], which turns hardware problem into software problems, are the most common technologies to develop systems that can automatically identify and demodulated many kinds of signals, but the power consumption of those systems is impossible to control under our requirement at the present time. Material [6 7 8] presents a novel method for using a same receivers structure basing on adaptive filter to demodulate FSK, PAM and QAM signals, and it is apparently used in military communication and involving at least 40 samples per symbols, so our concern of low power consumption cannot achieve by so high rate of oversampling and computing. Common receiver structures with configurable filters and oscillators are also solutions to demodulate different kinds of signals, as in [9]. However, those solutions necessitate using many multipliers to implement filters and it hard to reduce power consumption.

Based on the analysis of the ordinary MSH modem developed by HCF, we present a low-power receiver structure for multi-speed HART which can convergence fast and adaptively demodulate input signal modulated in non-coherent HART FSK or coherent HART C8PSK. The structure reduces power consumption by reducing the multiplications needed to demodulate a symbol. On the other hand, it saves the hardware resources by reusing them.

The rest of the paper is organized as follows. In section 2, we describe the work of HCF on MSH, and analyze it briefly. Section 3 dedicates to the proposed receiver structure. In section 4, analysis and simulations of the whole system are presented. At last, we conclude our work in section 5.

2. Analysis of former work

During 1995 to 2001, the HCF had developed a MSH modem, which did not apply in industry because the total worst case current was high up to 1.69 mA (should lower than 1 mA for safety sake). The receiver structure is shown in figure 1.

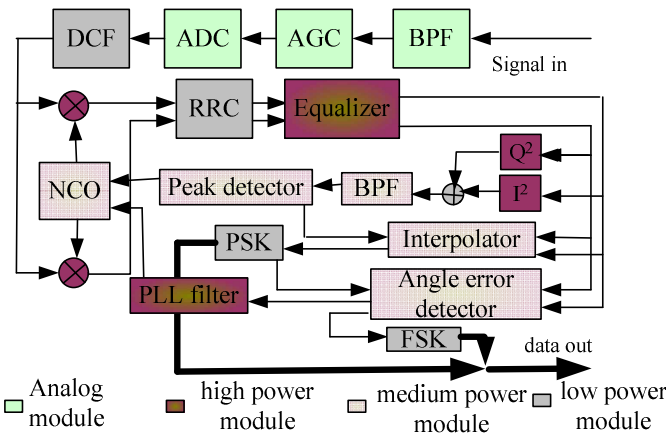


Figure1. Receiver structure of MSH developed by HCF

The whole system is initialized as the coming signal is modulated in C8PSK. The timing circuit of C8PSK will detect periodic peaks if the input signal is modulated in C8PSK; otherwise, the peak detector finds no peaks at all. If the input signal is modulated in FSK, the NCO is set to fixed frequency

of 1700 HZ, while the interpolator and PSK together are configured as a delay of a sample time. The NCO shifts the two FSK frequencies to ±500 H. The RRC (root raised cosine) filter designed as C8PSK shape filters can be reused here as a lowpass filter to remove the unwanted high frequencies. Angle detector designed for C8PSK carrier recovery can work as a slope detector for FSK. When C8PSK signals are received, it is obvious that the receiver structure can work as a typical coherent 8PSK receiver.

The MSH receiver structure by HCF has many advantages, but there several drawbacks that induce high power consumption and performance degeneration. HART channel is sketchily classified into 3 kinds according to the pole frequency of its lowpass filter model. The preset equalizer is implemented with complex multipliers, which work at 9 times of symbol rate, and its power consumption accounts for nearly 40% of the total. Though the angle detector works once per symbol in demodulating C8PSK signals, the PLL filter works at 9 times of symbol rate to prevent large fluctuations and shorten the settling time of the loop. Power consumption of the PLL circuit occupies nearly 40% of the total. Additionally, the timing loop works at 9 times of symbol rate too. Even so, the minimum C8PSK preamble length is 58 symbols, while the C8PSK preamble length is 40 symbols. Last but not least, the C8PSK angle detector uses the pre-interpolated samples other than the interpolated ones to compute angle errors in order to be compatible with FSK.

The major reason for high power consumption in the structure mentioned above is too many multiplications used per symbol demodulation, and the multiplier also results in large area in the chip. On the other hand, ordinary DPLL circuit cannot satisfy the synchronization requirements and new synchronization algorithms must develop to achieve better performance.

3. Low-Power Receiver structure for MSH

The proposed MSH receiver structure is shown as figure 2. The sample rate of the ADC is 25600Hz, and RRC filter is the same with HCF's scheme. As described in [10], unsynchronized clock arise due to many reasons, so time and phase synchronizers must be included in a MSH receiver.

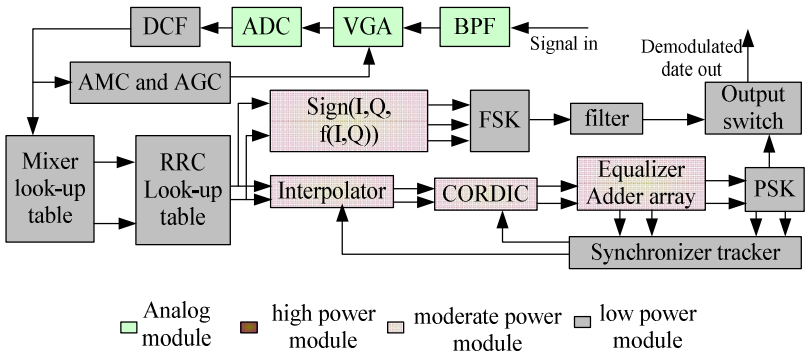


Figure2. Proposed MSH receiver structure

When AMC (automatic modulation classification) detects FSK signal, the mixer is set to fixed frequency 1600HZ. The detail demodulation algorithm of FSK will be discussed in section 3.3. When AMC detects C8PSK signal, mixer is set to fixed frequency 3200HZ. Interpolator, CORDIC (coordinate rotation digital computer), and equalizer only work twice per symbol. Equalizer adder array is used for synchronizer initialization for about 20 symbols time during preamble, and works as equalizer after synchronizer initialization finishes. It is controlled by the output of CDS (canonic signed-digit) confidents ROM as discussed in section 3.1 and 3.2. Synchronizer tracker reuses $\sin(\pi/8)$ and $\sin(3\pi/8)$ look up tables, and works once per symbol, as discussed in section 3.2. The detail route flow of MSH receiver will be discussed in section 3.4.

3.1 Equalizer for HART C8PSK signal

As mentioned in section 1, HART C8PSK signal must be equalized to be correctly demodulated. The wire channel of HART is relatively fixed, so preset equalizer can satisfy the requirements. According to experimental tests and the equalizer parameters of HCF MSH, HART channel equalizer with odd number of coefficients has characteristics that the module of center complex coefficient is more than 13 times bigger than that of others, and the phase of the center complex coefficient is small and close to zero. For example, when the pole frequency of the HART channel is 4000 HZ, the complex coefficients of a 7 order equalizer are shown as follow:

[0.0040, -0.0094, -0.0191, 1.0264, -0.0076, 0.0025, -0.0000]+ i*[-0.0040, 0.0174, -0.0489, -0.0768, 0.1596, -0.0521, 0.0112].

According to this characteristic of the preset equalizer, using CSD coefficient filter structure to implement the equalizer will greatly decrease power consumption. For example, we can normalize the center complex coefficient to 1 and use CSD coding the above set of coefficients, then we get

[00000000010001, 00000000-10-10-10, 0000000-10010-1, 10000000000000, 0000000-10-10010, 00000000011001, 00000000000-101] +
[00000001000010, 00000001000010 00000-10100-1000 00000000000000, 00001001000-100 00000-1010-10010 00000000101100]*i

From the above CSD coded coefficient, we can conclude that a 12 bits multiplier can be replaced by 3 adders with 3 shift register, so the power consumption can be greatly decreased. We introduce a novel type of equalizer for MSH as show in figure 3.

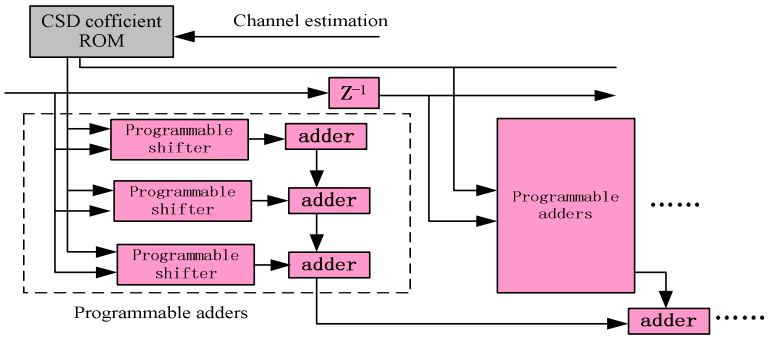


Figure3. CSD coded preset equalizer

As discussed in section 3.2, the equalizer works twice per symbol, so power consumption can decrease further; equalizer adder array and shift registers are reused to carry out sliding windows addition for synchronizer initialization, so area cost can decrease.

3.2. Synchronization for C8PSK signal

As mentioned in section 1, ordinary DPLL or DPLL with gear-shift algorithms cannot converge in short time, while synchronization algorithms that use autocorrelation need too many multiplications, so they induce higher power consumption. Reference [11] provided a novel fast synchronization algorithm for HART C8PSK carrier recovery and symbol timing with detail proofs, and two propositions will be used here without proving.

Synchronizer initialization

Digital signal of HART C8PSK output from the receiver shape filter RRC can be written as:

$$Q(n) = \sum_i g(nT_S - iT + \tau)\cos(\varphi_i + \Delta\theta) + N_Q(n) \quad (1)$$

$$I(n) = \sum_i g(nT_S - iT + \tau)\sin(\varphi_i + \Delta\theta) + N_I(n) \tag{2}$$

$$\Delta\theta = \theta_T - \theta_R \tag{3}$$

Where $Q(n)$ is the quadrature component, $I(n)$ is the in-phase component; θ_T represents the phase of transmitter carrier and θ_R is the phase of receiver carrier; $\Delta\theta$ is carrier phase error including the small frequency offset of the carrier; φ_i is the symbol phase for transmitted messages; $\tau < 0.5 * T_S$ is timing error; T is symbol period; $T_S = T/8$ is sampling period; $g(n)$ represents the combined impulse response of shape filter, analog profiler and channel; $N_Q(n)$ and $N_I(n)$ are noise. HART C8PSK PHL specifies the carrier frequency shall fluctuate within 3200±1 Hz at both transmitter and receiver end, so the frequency mismatch can be negligible here. Defining

$$SumQ(m) = \sum_{n=1}^{16} Q(n+m) \quad SumI(m) = \sum_{n=1}^{16} I(n+m) \quad ; \tag{4}$$

$$Ti(m) = \sum_{n=1}^{8} I(n+m) - \sum_{n=8}^{15} I(n+m) \tag{5}$$

Proposition 1: During the preamble of HART C8PSK (except the first and last 3 symbols of the preamble), $SumQ(m)$ and $SumI(m)$ can be written as:

$$SumQ(m) = A\cos(\Delta\theta) \quad ; SumI(m) = A\sin(\Delta\theta)$$

Proposition 2: During the preamble of HART C8PSK (except the first and last 3 symbols of the preamble), if carrier phase is eliminated or small, and $Ti(q)$ is the nearest point to zero, then $Ti(q) \approx B\tau$

During the preamble, synchronizer initialization algorithm of C8PSK is described as follow

(a) Sliding windows addition as (4) are calculated and the results go through mean filter;
(b) defining $\Delta\theta$ =45*k+m; the result $SumQ(m)$ and $SumI(m)$ go through the PSK judgment module, which judge the function parameter k; a little lookup table of abstract value $SumQ(m)$ is used to compute m;
(c) Feed back $\Delta\theta$ to CORDIC to correct carrier phase error; CORDIC works at sampling rate for timing initialization, and working rates is turned down to twice per symbol when timing initialization finishes ;
(d) Sliding windows addition as (5) is calculated; choose $Ti(q)$ that nearest to zero, and calculate timing offset τ . Feed back q and τ to Farrow interpolator.

Equalizer starts after synchronizer initialization finishes, so sliding windows additions can be carried out using equalizer adder array and shifter when every CSD coefficient ROM outputs proper coefficients for programmable adder array module.

Synchronizer tracking

The offsets of timing and carrier phase are relative small and stable in short time, so they have little influence to symbol demodulation in short time. On the other hand, equalizer and interpolator are high

power component, so reducing their computing rate is an effective way to lower power consumption. Fractionally spaced equalizer can work well with timing error. Therefore, to guarantee the performance of the system, T/2 spaced equalizer is adopted. We can get two equalized samples per symbol if the equalizer works at this lowest computation rate.

The timing offset is computed using Gardener algorithm:

$$eT(nT) = I_p(nT)*[I((n+1/2)T) - I((n-1/2)T) + Q_p(nT)[Q((n+1/2)T) - Q((n-1/2)T)] \tag{6}$$

The carrier phase offset is computed as:

$$eC(nT) = Ip(nT)*Q(nT) - I(nT)*Qp(nT) \tag{7}$$

Where $Ip(nT)$ and $Qp(nT)$ are known preamble during training sequence, and judgment feedbacks during the demodulation of the useful message; $I(nT)$ and $Q(nT)$ are samples from the equalizer. From (6) and (7), we can see that timing offset and carrier offset are calculated in different period of a symbol and the multipliers can be implemented with time divided used lookup tables, because the absolute values of $Ip(nT)$ and $Qp(nT)$ are sin(π/8) and sin(3π/8).

Timing offset is fed back to interpolator, which can work twice per symbol as equation (6) and (7) imply. If carrier phase offset is fed back to mixer as reference [11] and HCF did, the mixer must be implemented with two multipliers, and phase recovery loop introduces RRC large loop delay. Carrier phase offset is feed back to a pipeline CORDIC circuit between the equalizer and PSK judge to compensate phase offset as shown in figure 2.

3.3. demodulation algorithm for FSK

The mixer is set to fixed frequency 1600 Hz when FSK signal is detected by AMC module. When a FSK symbol 1 (1200 Hz signal) is transmitted, receiver mixer produces a -400Hz signal and a +2800Hz signal; while for a FSK symbol 0 (2200 Hz signal), it produces a +600Hz signal and a +3800Hz signal (+ and – represents the rotate orientation, anticlockwise or clockwise). The RRC filer used for C8PSK is a lowpass filter with pass frequency at 1600Hz and stop frequency at 2400Hz, so the output signal from RRC is a -400Hz signal for FSK symbol 1 or a +600Hz signal for FSK symbol 0, both of which are constant envelop. For a -400Hz constant envelop signal, the adjacent two samples has a -6°phase error; while for a +600Hz signal, the phase error is +9°.

Defining

$$f(I_n, Q_n) = (abs(I_n) - abs(I_{n-1}) - abs(Q_n) + abs(Q_{n-1}))*sign(Q_n)*sign(I_n) \tag{8}$$

Where I_n, I_{n-1} and Q_n, Q_{n-1} are in-phase components and quadrature components of adjacent two samples respectively. It is easy to know that $f(I_n, Q_n)$ <0 when signal frequency<0, and $f(I_n, Q_n)$ >0 when signal frequency>0. For HART FSK demodulation, the amplitude of $f(I_n, Q_n)$ is large than 10 percent of the amplitude of the received, so 5 bits precision is enough. The sign of I_n, Q_n can be used to judge axis crossing. FSK module makes demodulation judgment according to the sign of I_n, Q_n, and $f(I_n, Q_n)$. The subsequent filter filters out the interface of noise.

3.4. route flow of MSH receiver

Though AMC (automatic modulation classification) and channel estimation are implanted with high power algorithms, such as FFT [12] and wavelet transformation [13], a joined design of AMC and channel estimation was described in Reference [14], so we will not spread them out here. When HART carrier is detected, the mixer is set to fixed frequency 3200 Hz, so mixer should mix input samples with sin(k* π /4) and cos(k* π /4) signals (k is integer). According to the periodic of sinusoidal signal, only sin(π /4) lookup table is needed to carried out the mixing frequency.

First, channel estimation and AMC are carried out, and synchronizer initialization described in section 3.2 is carried out concurrently. AMC finishes after about 160 samples. If AMC detects FSK signal, synchronizer initialization results are meaningless and abandoned. C8PSK circuits stops working, FSK circuits starts, and mixer set to fixed frequency of 1600 Hz. Mixer should mix input samples with sin(k* π /8) and cos(k* π /8) signals (k is integer). So sin(π /8), sin(π /4), and sin(3 π /8) lookup tables are needed. FSK circuits work as described in section 3.3.

If AMC detects C8PSK signal after the first 160 samples, synchronization tracking circuits set the results of synchronizer initialization to CORDIC and interpolator and start to work. CSD coefficients ROM outputs a set of equalizer coefficients according to the result of channel estimation, so the equalizer adder array works as preset equalizer. Then the C8PSK circuits work as ordinary 8PSK demodulator, but with a good synchronizer initial parameters, so the MSH receiver can work stably.

4. Analysis and simulation of the proposed structure

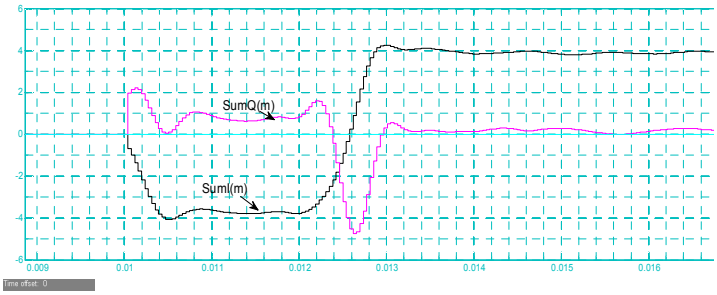
In integrated circuit, a multiplication consumes considerably more power compared to a addition, while the power of a table looking-up is negligible compare to a multiplication or a addition. Table 2 shows the computation operations per symbol demodulation of our receiver structure and a normal one.

Table 2. comparation computation operations per symbol demodulation

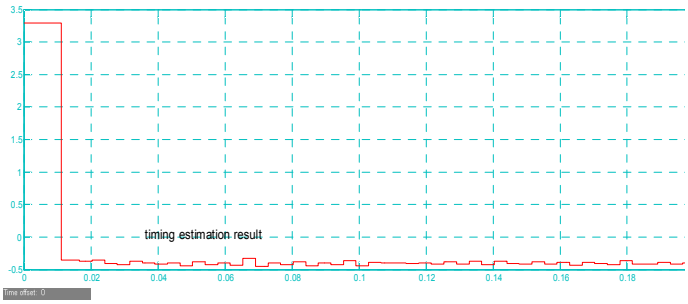
Items for comparation		**multiplication**	**addion**	**Table looking-up**
Per C8PSK symbol	proposed stucture	6	78	146
	Normal stucture as HCF	>130	>80	>140
Per FSK symbol	proposed stucture	0	212	336
	Normal stucture as HCF	>70	>170	>310

There are several reasons for the above results: (1)the structure of preset equalizer has been optimized, (2) working frequency of high power components—equlizer and interpolator, decreases from 9 times to 2 times per symbol demodulation; (3)sample rate of ADC is 8 time of symbol rate for C8PSK, so the frequency mixing(usually implemented with 2 multipliers) is implemented with a look-up table; (4) the proposed FSK algorithm is a frequency discrimination in essence, but it does not use multiplications as normal algorithms as HCF used. (5) RRC table is 12.5% smaller than that in HCF scheme.

Computer simulations are performed to verify the performance of the proposed MSH receiver structure. Signed fixed-point arithmetic is used throughout simulation. Number precision of the MSH is as follow: 8 bits for A/D converter; 8 bits addresses and 7 bits precision lookup table for sin(π /8), sin(π /4), and sin(3 π /8)lookup tables; 18 central symmetric lookup tables for RRC, each table has 7 bits addresses and 8 bits precision; each of the equalizer adders has 10 bits precision and the output result precision reserves the high 8 bits; According to HCF, HART receiver should be able to work under SNR=17 circumstance, while we add 14db noise to signals in simulation. In case of the HART channel pole frequency at 4000HZ, Simulation results are shown as figure 4, 5, and 6.

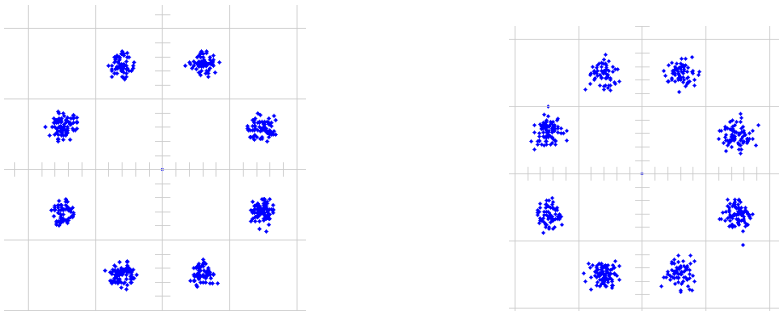


(a) SumQ(n) and SumI(n)



(b) timing estimation

Figure 4. Synchronization result of HART C8PSK
(note: the time period of (a) and (b) are different in figure 4)



(a) Phase error feed back to CORDIC (b) Phase error feed back to mixer

Figure 5. Scatter spot of HART C8PSK

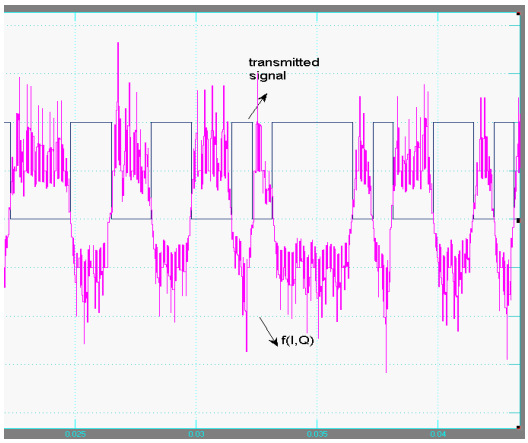


Figure 6. $f(I_n, Q_n)$ in FSK demodulation

Figure 4 shows the process and the result of synchronization. As we can see form figure 4(a), course phase estimation in the sight of $SumQ(m)$ and $SumI(m)$ fluctuates because of noise and channel distortion (equalizer does not start in synchronizer initialization), so carrier recovery initialization algorithm just provides a course estimation of phase. Timing offset estimation is shown in figure 4(b) and we can see that initialization algorithm finds the q and τ for the interpolator first, so there is a big step at the beginning of the estimation. As shown in figure 4, synchronizer initialization can finish in less than 20 symbols, with little synchronization error.

Figure 5 shows the scatter spot of C8PSK demodulation, and we can see that figure 5(a) convergences better than figure 5(b). Feeding back phase error to CRODIC avoids the big delay of RRC, so the carrier phase compensation loop has smaller loop delay than HCF structure and reference [11]. Smaller loop delay leads to smaller phase error and better convergence.

Figure 6 shows the demodulation process of FSK. As shown in figure 6, absolute values of $f(I_n, Q_n)$ become small at the transition region of two different symbols, and this is low pass filter effects of RRC. It has no effects to FSK demodulation, because we use $sign(f(I_n, Q_n))$ for judgment and timing extraction.

5. Conclusion

In this paper we have presented a low-power digital receiver for MSH. Synchronizer is divided into initialization stage and tracking stage. In first stage, it reuses the equalizer adders and employs the preamble to quickly attain equilibrium state; in tracking stage, it is time-divided carried out and reduces the computation rate of the equalizer and interpolator. The proposed CSD coded preset equalizer not only saves power per operation, but also facilitates resource reusing. For HART FSK signal, a novel demodulation algorithm is introduced which reuses the modules for demodulating HART C8PSK signal. The proposed algorithm only introduces 3 adders and a little logic resource on basis of the original structure, but its power decreases greatly.

The whole structure reduces power consumption by reducing the multiplications needed to demodulate a symbol. On the other hand, it saves the hardware resources by reusing them. Computer simulations results show that the proposed MSH receiver structure can convergence quickly and work very well in low SNR.

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