Low Complexity Synchronization Algorithms for HART C8PSK

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Abstract. This paper not only describes novel fast synchronization algorithms for HART C8PSK carrier recovery and symbol timing, but also provides a solution for HART C8PSK low power design. Synchronization is divided into two parts: initialization and tracking, the former part of which uses novel algorithms to attain equilibrium state quickly, and the later part of which is time-divided carried out. On basis of the proposed algorithms, high power component—equalizer and interpolator, can work at lowest rate, which indirectly reduces the system power. The implementation of those algorithms needs no additional hardware resource except a few lookup tables, and at the same time, they add negligible power consumption to the whole system. Simulations showed that the proposed synchronization algorithms can work very well in low SNR.

Keywords: Fast synchronization algorithms, low power design, HART C8PSK, Low Complexity.

1 Introduction

The HART (Highway Addressable Remote Transducer) Protocol is the global standard for sending and receiving digital information across analog wires between smart devices and control or monitoring system. The global installed base of HART-enabled devices is the largest of all communication protocols at more than 20 million. Because digital communication rate of the existing HART FSK protocol limits the use the HART, the HCF (HART communication Foundation) established the HART C8PSK (Coherent 8-way Phase Shift Keying) PHL (Physical Layer) Specification, which can provide 8-10 times higher digital rate [1]. In order to be intrinsic safe, HART has strict requirement on power dissipation, and HART C8PSK is significantly more complex signal than HART FSK, so the low power design of the HART C8PSK is very tough. An Austria company, called Volker Schindler, developed the first C8PSK HART modem chip by using lower power semiconductor technology in 2009, the current of which was 800uA, smaller than 1000uA requirement, but still larger than 750uA, the applicable level [2].

HART belongs to burst communication. HART C8PSK PHL specifies that receiver should adopt coherent demodulation, so rapid recovery of carrier phase and timing is

L. Jiang (Ed.): International Conference on ICCE2011, AISC 110, pp. 661–669.
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essential. Short cyclic preamble is provided for channel estimation and synchronization. Digital phase-locked loop (PLL) with gear-shift algorithms can adjust the bandwidth of the PLL to solve both problems of fast acquisition and jitter reduction, so they are always solutions for this kind of problems [3, 4]. However, using the above technology, some industry giant, such as Rosemount, SMAR, and Siemens, organized by HCF, developed a HART C8PSK modem in 1998, only to find that the receiver need at least 58 preambles to stabilize and the power consumption of the loop was 569uA [5]. So techniques developed from DPLL, such as dual-loop DPLL [6], have difficulties in controlling the power dissipation in HART C8PSK synchronization. Huang Introduced a fast carrier synchronization algorithm for MPSK based on Mth power loop [7], but this kind of algorithm needs fine timing and high SNR, additionally it is hard to control power too. Based on a very short special carrier preamble modulated by a known pattern, Andronico introduced an algorithm to fast estimate synchronization parameters, but six complex multiples were involved [8]. Synchronization algorithms used in OFDM system always employ signal autocorrelation to get timing parameters fast, but they do not consider the carrier phase offset.

In this paper, we present novel algorithms with low complexity for HART C8PSK to fast estimate the synchronization parameters. The estimation is carried out before the equalizer and interpolator start working, and involves no multipliers. During the synchronization tracking, time-divided algorithms are used and they need low sampling rate which reduces the computation rate of high power components such as equalizer and interpolator.

In section 2 below, a brief description of the whole C8PSK receiver system is given. Section 3 dedicates to initialization algorithms for synchronization. Section 4 describes synchronization tracking. In section 5, simulation results of the proposed algorithms are presented. At last, we conclude our work in section 6.

2 Background

HART FSK underlies Bell-202 Telecomm standard, while HART C8PSK is similar to the signaling specified in the CCITT V.27 telecommunications standard, using a higher number of symbols per second and a wider bandwidth than V.27. HART C8PSK employs eight phases of a 3200 HZ carrier to transmit digital signals, and the preamble is 40 cyclic symbols of symbol 6(67.5°) and symbol 2(-67.5°). Symbol rate of HART C8PSK is 3200HZ. The receiver structure is shown as figure 1.

It should be noted that the equalizer is a preset CSD coded equalizer as shown in figure 2, which is made up of programmable shifters and adders. Those programmable shifters work according to a set of coefficients in the CSD coefficient ROM, which is decided by the result of channel estimation. When HART C8PSK signal is detected, channel estimation and synchronization initialization are carried out in parallel first. Equalizer and interpolator will not work until they finish. The adders of the equalizer are used for synchronization initialization as described in the next section. The sample rate of the ADC is 25600Hz, this is, 8 samples in a symbol time.

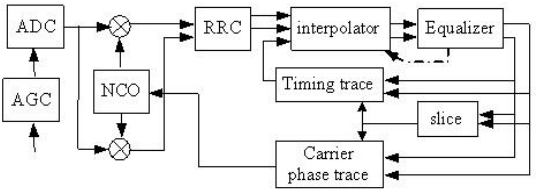

Fig. 1. Receiver structure

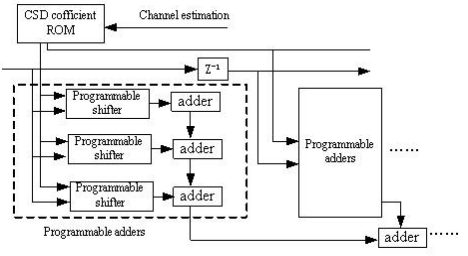

Fig. 2. CSD coded preset equalizer

3 Initialization of Synchronization

Synchronization initialization starts working after the AGC finish initialization, and uses the samples output from the RRC filters. Initialization algorithms reuse the adders and shift registers of equalizer for implementation.

Periodic preamble sent by HART C8PSK transmitter turns out periodic preamble signal to HART channel. The time for signal detection and AGC initialization is longer than combined impulse response of channel and shape filter, so the signal input to the initialization circuits can be seen as periodic signal. Digital signal of HART C8PSK output from the receiver shape filter (RRC) can be written as:

$$Q(n) = \sum_i g(nT_s - iT + \tau)\cos(\varphi_i + \Delta\theta) + N_Q(n) \tag{1}$$

$$I(n) = \sum_i g(nT_s - iT + \tau)\sin(\varphi_i + \Delta\theta) + N_I(n) \tag{2}$$

$$\Delta\theta = \theta_T - \theta_R \tag{3}$$

Where θ_T represents the phase of transmitter carrier and θ_R the phase of receiver carrier; φ_i is the symbol phase for transmitted messages; τ <0.5* T_S is timing error; T is symbol period; T_S =T/8 is sampling period; $g(n)$ represents the combined

impulse response of shape filter, analog prefilter and channel; $N_Q(n)$ and $N_I(n)$ are noise. HART C8PSK PHL specifies the carrier frequency shall fluctuate within 3200±1 Hz at both transmitter and receiver end, so the frequency mismatch can be negligible here. Defining

$$SumQ(m)=\sum_{n=1}^{16}Q(n+m)\quad SumI(m)=\sum_{n=1}^{16}I(n+m) \tag{4}$$

;

3.1 Proposition for Carrier Phase Estimation

Proposition 1: During the preamble of HART C8PSK (except the first and last 3 symbols of the preamble), $SumQ(m)$ and $SumI(m)$ can be written as:

$$SumQ(m)=A\cos(\Delta\theta)\quad ;SumI(m)=A\sin(\Delta\theta)$$

Prove: The preamble of the C8PSK are cyclic symbol 6 and symbol 2 which can be viewed as a 1600 Hz periodic signal. Shape filter, analog prefilter and channel can filter out or distort some components but can not change the periodicity, so there are 16 samples in a period. AWGN noise is ignorable in the accumulation, so we can get that

$$SumQ(m)=\sum_{n=1}^{16}Q(n+m)=\sum_{n=1}^{16}Q(n)$$

$$=\sum_{n=1}^{16}\sum_{i}\{g[nT_s-(2i-1)T+\tau]\cos(67.5+\Delta\theta)$$

$$+g(nT_s-2iT+\tau)\cos(-67.5+\Delta\theta)\}$$

$$=\sum_{n=1}^{16}\sum_{i}\{\{g[nT_s-(2i-1)T+\tau]+g(nT_s-2iT+\tau)\}$$

$$*\cos 67.5*\cos\Delta\theta-\{g[nT_s-2(i-1)T+\tau]-g(nT_s-2iT+\tau)\}*\sin 67.5*\sin\Delta\theta \tag{5}$$

Defining

$$X(i,\tau)=\sum_{n=1}^{16}\sum_{i}g(nT_s-iT+\tau) \tag{6}$$

For $T_S=\mathrm{T}/8$, it is obviously that

$$X(i,\tau)=X(i+1,\tau) \tag{7}$$

So it is easy to get

$$X(2i,\tau)=X(2i-1,\tau) \tag{8}$$

Then the second half of (5) equals 0, and the first half is

$$SumQ(m)=2X(2i,\tau)*\cos 67.5*\cos\Delta\theta \tag{9}$$

For the same reason, we can get

$$SumI(m) = 2X(2i,\tau) * \cos 67.5 * \sin \Delta\theta \tag{10}$$

Proposition 1 is proved.

3.2 Proposition for Timing Phase Estiamtion

Defining

$$Ti(m) = \sum_{n=1}^{8} I(n+m) - \sum_{n=8}^{15} I(n+m) \tag{11}$$

Proposition 2: During the preamble of HART C8PSK (except the first and last 3 symbols of the preamble), if carrier phase is eliminated or small, and $Ti(q)$ is the nearest point to zero, then $Ti(q) \approx B\tau$

Prove: Substituting $\Delta\theta = 0$ into (2), we can see that $I(n)$ is the result of a cyclic sin67.5 and sin-67.5 series signal filtered by a low-pass filter (RRC), so it is easy to deduce that $I(n)$ is still a 1600HZ period signal. For the same reason, $Q(n)$ approximates a direct current signal.

Taking no account of ISI introduced by the channel, we can see that the best timing sample happens when $\tau = 0$ and $nT_s = iT$.

For periodic signal $I(n)$, Reference [10] has proved that $Ti(m)$ is a monotone function during in a cyclic of two symbols and equals 0 at the best sample time.

From reference [11], we can get that the coupling of carrier phase and timing phase is very small around the stable point $Ti(q) = 0$. Since the timing error τ is less than 1/16 of symbol time here, from the linearization of (4) we get our conclusion. Proposition 2 is proved.

3.3 Initialization Algorithm

Since synchronizer initialization algorithms reuse the C8PSK judgment module, we describe C8PSK judgment algorithm first. HART C8PSK judgment algorithm carries out in three steps: abstract values and signs of $I(nT)$ and $Q(Tn)$ output from the equalizer are computed first; then compare the abstract values; the result the comparing and the two signs are input to a 3-8 decoder to judge which symbol is received.

Based on proposition 1 and 2, synchronizer initialization algorithm of Multi speed HART is described as follow

(a) Sliding windows as (4) are calculated and the results go through mean filter;

(b) defining $\Delta\theta$ =45*k+m; the result $SumQ(m)$ and $SumI(m)$ go through the PSK judgment module, which judge the function parameter k; a little lookup table of abstract value $SumQ(m)$ is used to compute m;

(c) Feedback $\Delta\theta$ to oscillator to correct carrier phase error; wait three symbol time and begin timing phase estimation;

(d) Sliding windows as (11) are calculated; choose $Ti(q)$ that nearest to zero, and calculate timing offset τ ; Feedback q and τ to Farrow interpolator.

4 Synchronization Tracking

Synchronization initialization provides coarse parameters estimation and only takes about 15 preambles to be done. It is necessary to use the equalized preambles to get better estimation of synchronization parameters. Additionally, the length of HART messages varies from several bytes to hundreds of bytes. In order to get better bit error rate, decision feedback synchronization are used for parameters tracking, employing digital PLL with gear-shift algorithms.

Equalizer and interpolator are high power component, and reduce their computing rate is effective way to lower power consumption. Fractionally spaced equalizer can work well with timing error. Therefore, to guarantee the performance of the system, T/2 spaced equalizer is adopted. We can get two equalized samples per symbol if the equalizer works at this lowest computation rate.

The timing offset is computed using Gardener algorithm:

$$eT(n) = I_p(n)*[I(n+1/2) - I(n-1/2) + Q_p(n)[Q(n+1/2) - Q(n-1/2)] \quad (12)$$

The carrier phase offset is computed as:

$$eC(n) = I_p(n)*Q(n) - I(n)*Q_p(n) \quad (13)$$

Where $I_p(n)$ and $Q_p(n)$ are known preamble during training sequence, and judgment feedbacks during the demodulation of the useful message; $I(n)$ and $Q(n)$ are samples from the equalizer. From (12) and (13), we can see that timing offset and carrier offset are calculated in different time of a symbol period and the multipliers can be implemented with time divided used lookup tables.

Both of the two offsets are filtered by one order lowpass filters before sending to oscillator or interpolator. The pole frequency of the lowpass filters decrease at the transition form preamble to useful data.

5 Analysis and Simulation

The proposed synchronization algorithms do not use multipliers, or any other complex computation resources. During the initialization phase, each sliding window of (4) and (11) needs only 2 additions for a sample output from the RRC filter, and they do not affect the maximum power of the system because equalizer and interpolator do not work at that time. During the tracking phase, only four additions and four table lookups are needed for the two offsets estimation in a symbol, and power consumption of those operations is negligible compared with that of equalizer. Further more, equalizer and interpolator can work at their lowest rate based on the proposed algorithms.

Computer simulations were performed to verify the performance of the proposed synchronization algorithms. Signed fixed-point arithmetic was used throughout simulation. The number precision of the receiver is as follow: 8 bits for A/D converter; 9 bits addresses and 10 bits precision lookup table for NCO; 18 central symmetric lookup tables for RRC, each table has 7 bits addresses and 8 bits precision; each of the equalizer adders has 10 bits precision and the output result precision reserves the high 8 bits. According to HCF, HART receiver should be able work under SNR=16 circumstance, while we add 13db noise to signals in simulation. Figure 3, 4, 5, and 6 are simulation results of the proposed algorithm.

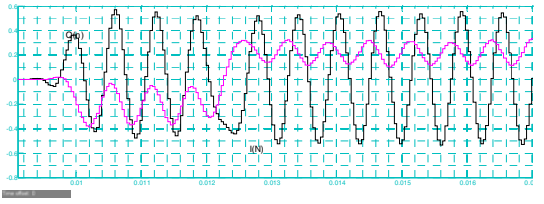

Fig. 3. Q(n) and I(n) from RRC (before equalizer)

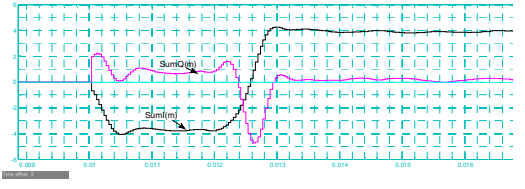

Fig. 4. SumQ(n) and SumI(n) output from equalizer

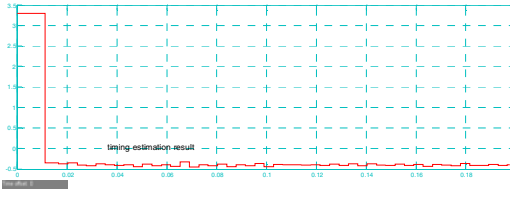

Fig. 5. The result of timing estimation

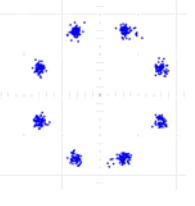

Fig. 6. scatter plot of the C8PSK receiver

Figure 3 shows the signal output from RRC filter, and we can see that there exists a great phase offset at the beginning of the simulation. As shown in figure 3, there still exists some phase offset when course carrier phase compensation carries out. Figure 4 shows the process and the result of course phase estimation in the sight of $SumQ(m)$ and $SumI(m)$, then we can see that $SumQ(m)$ and $SumI(m)$ fluctuate because of noise, so carrier recovery initialization algorithm just provides a course estimation of phase offset. Timing offset estimation is shown in figure 5 and we can see that initialization algorithm finds the q and τ for the interpolator first, so there is a big step at the beginning of the estimation. As shown in figure 5, timing tracking eliminates little offset and fluctuates because of noise. From figure 6, we can see that all the demodulated symbols have very good convergence, except several symbols of 6 and 2(67.5 and -67.5), which are part of preamble used to get fast initialization for synchronization, so they have no influence on receiving of useful message.

6 Conclusion

In this paper we have introduced novel synchronization algorithms for HART C8PSK. Based on the structure of the HART C8PSK preambles, novel fast synchronization algorithms are introduced and proved for course parameters estimation. Tracking algorithms make the two estimation work in different phases of a symbol time, so lower power and resource reuse can be achieved. The implementation of those algorithms needs no additional hardware resource except a few lookup tables, and at the same time, they add negligible power consumption to the whole system. Simulations have shown that the proposed synchronization algorithms can work very well in low SNR. At last, the proposed algorithms can use in similar case too.

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